

Arithmetic Circuits of the Noisy-Or Models

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PGM'08, Hirtshals, Denmark

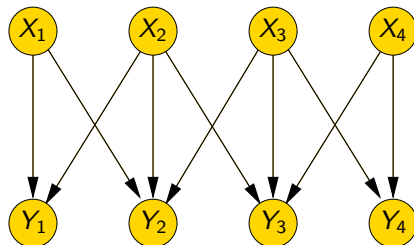
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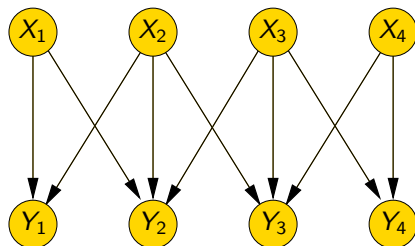
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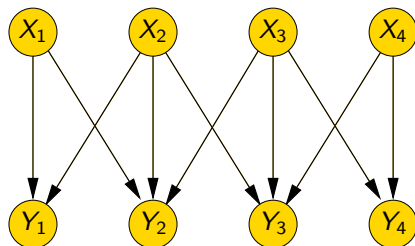
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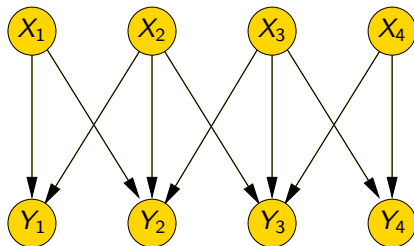


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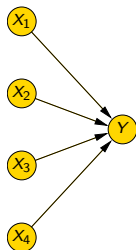
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- Y_i is false only if all its parents with value true are inhibited.

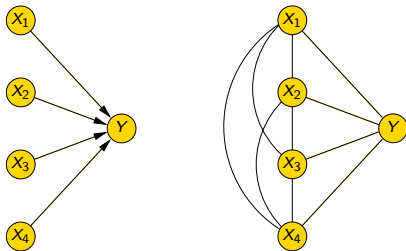
Compilation of a noisy-or gate - the standard BN approach

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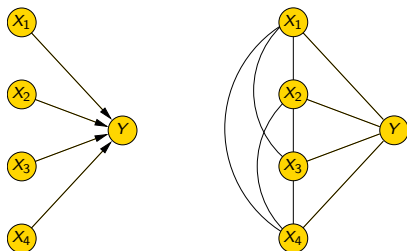
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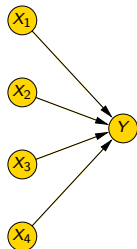
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The total table size is $2^5 = 32$.

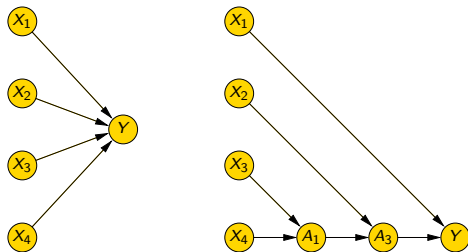
Compilation of a noisy-or gate - parent divorcing

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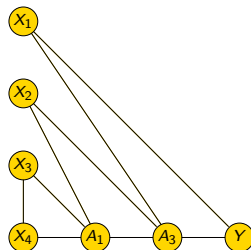
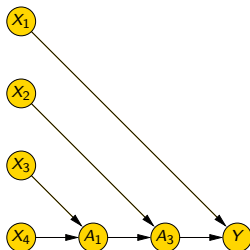
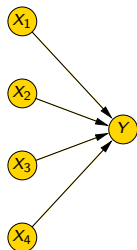
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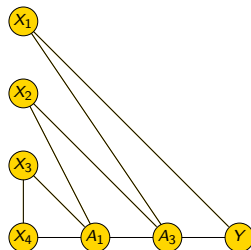
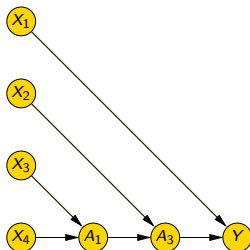
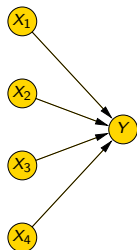
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The total table size is $3 \cdot 2^3 = 24$.

Rank-one decomposition

Díez and Galán (2003), Vomlel (2002), Savický and Vomlel (2007)

$$P(Y_i = y_i | X_{Pa(i)} = x_{Pa(i)}) = (1 - 2y_i) \prod_{j \in Pa(i)} p_{i,j}^{x_j} + y_i \prod_{i=1}^n 1$$

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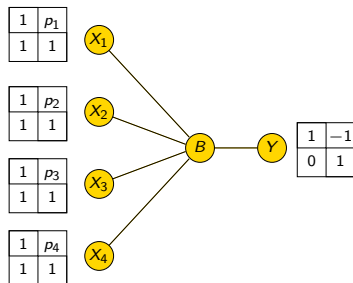
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Correspondence to tensor rank-one decomposition

Savický and Vomlel (2007)

A decomposition of a conditional probability table $P(Y|X_1, \dots, X_n)$ using the auxiliary variable B

$$P(Y_i|X_{Pa(i)}) = \sum_B \xi(B, Y_i) \cdot \prod_{j \in Pa(i)} \varphi_{i,j}(B, X_j)$$

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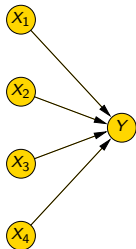
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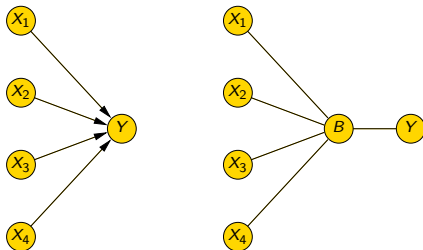
Definition (Tensor of rank one)

A tensor has rank one if it is the outer product of vectors.

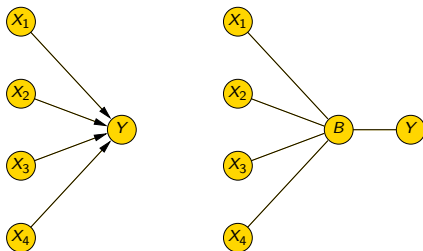
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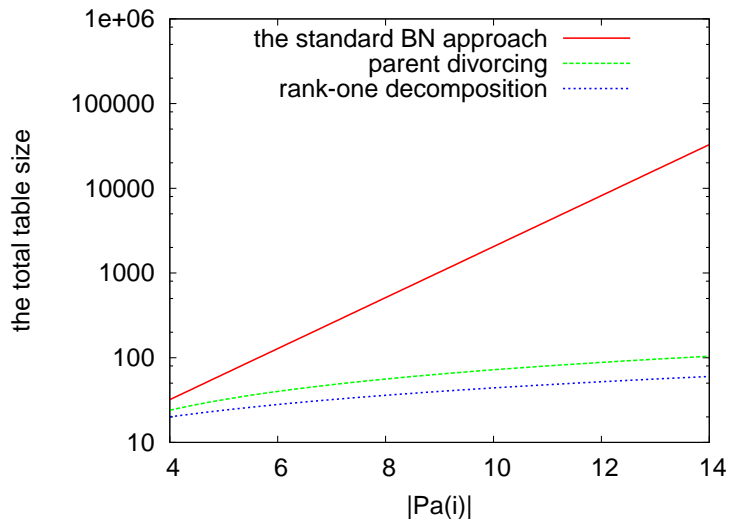


Compilation of a noisy-or gate - rank-one decomposition



The total table size is $5 \cdot 2^2 = 20$.

Comparisons for the noisy-or gate



Arithmetic circuits

Definition (Arithmetic circuit (AC))

An AC is a rooted, directed acyclic graph whose leaf nodes correspond to its inputs and whose other nodes are labeled with multiplication and addition operations. The root node corresponds to the output of the AC.

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$$\lambda_x = \begin{cases} 1 & \text{if state } x \text{ of } X \text{ is consistent with evidence } \mathbf{e} \\ 0 & \text{otherwise.} \end{cases}$$

If there is no evidence for X , then $\lambda_x = 1$ for all states x of X .

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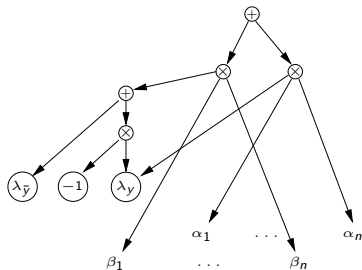
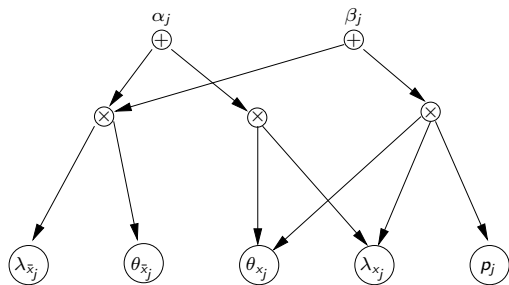
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Circuit output:

- **probability of evidence $P(\mathbf{e})$.**

AC of a noisy-or gate



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- The size of an AC (i.e. number of its edges) can be used as a measure of inference complexity

Arithmetic circuits (ACs) - Part II

- Darwiche et al. proposed two different methods for constructing ACs of BNs - **c2d** and **tabular** - both are implemented in a BN compiler Ace (by Chavira and Darwiche).

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- Ace uses the parent divorcing method for preprocessing noisy-or models.
- We use the size of ACs to compare the effect of preprocessing Bayesian networks by Ace's parent divorcing giving (what we call) the **original model** and by rank-one decomposition giving the **transformed model**.

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aligator.utia.cas.cz: 8x AMD Opteron 8220, 64GB RAM
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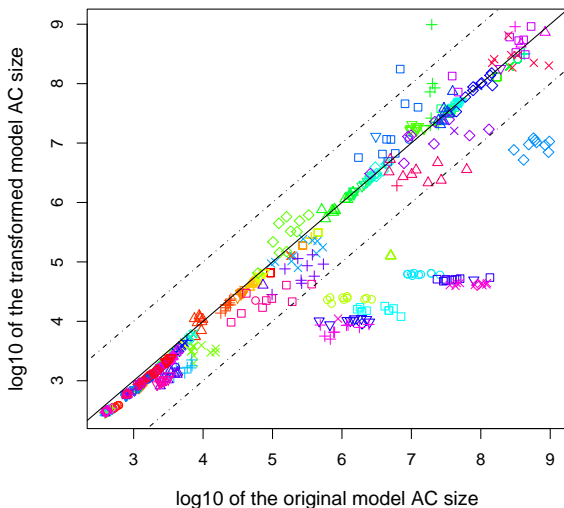
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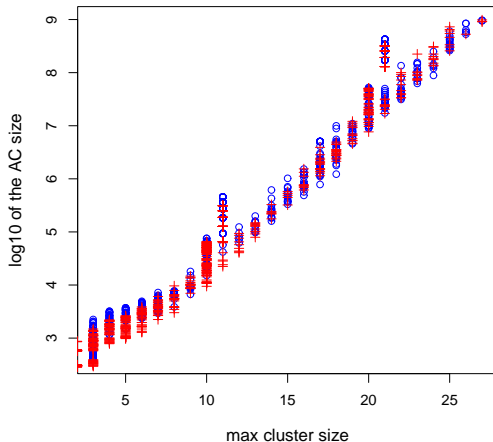
All models and results are available at:

<http://www.utia.cz/vomlel/ac/>

Transformed vs. original model AC size

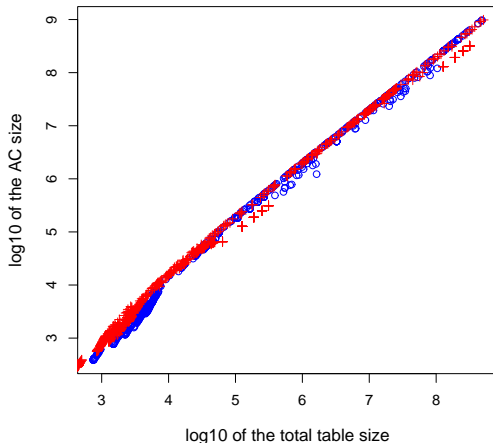


Dependence of the AC size on the size of a largest clique for the original and the transformed models

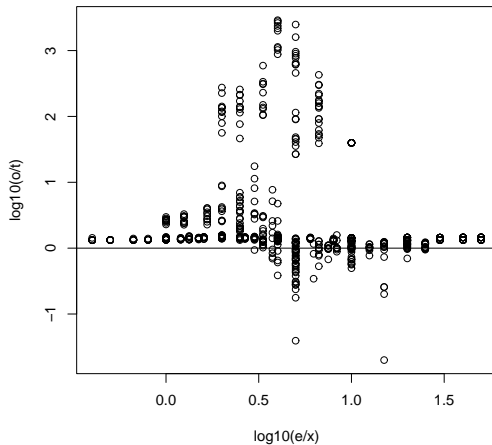


Dependence of the AC size on the total table size

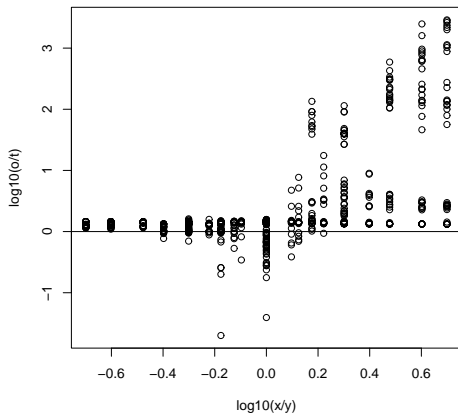
for the **original** and the **transformed** models



Dependence of the AC size reduction on the relative number of edges



Dependence of the AC size reduction on the ratio of the number of nodes in the first and the second levels



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- The AC size depends on the total table size in the resulting model.

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- We conducted additional experiments with all eleven models with significant loss in the AC size.
- In all of these cases we were able to reduce the deterioration factor to less than three using a better triangulation method provided by Hugin.